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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,626	11/30/2004	Bernardo De Oliveira Kastrup Pereira	NL02 0444 US	6975

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,626	DE OLIVEIRA KASTRUP PEREIRA, BERNARDO	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 12/20/2006.

Withdrawn Rejections

4. Applicant, via amendment, has overcome the 35 U.S.C. § 112, second paragraph, rejections set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeHon et al., U.S. Patent No. 5,956,518, (Herein referred to as DeHon) in view of Mirsky et al., U.S. Patent No. 5,915,123 (Herein referred to as Mirsky).

5. Referring to claim 1, DeHon has taught an integrated circuit comprising:

a plurality of processing elements *[basic functional units (BFUs); component 100]* for executing in parallel at least a subset of a plurality of instructions *[Fig. 4; column 5, lines 3-10, 44-48]*;

issuing means *[F BFUs; See Fig. 4]* for configuring the plurality of processing elements by issuing a program-counter-driven instruction flow *[from the PC BFU; See Fig. 4]* to the plurality of processing elements *[column 5, lines 16-23, 44-48]*; and

configurable interconnection *[programmable interconnect; component 101]* means for connecting each processing element from the plurality of processing elements to at least a subset of other processing elements from the plurality of processing elements *[Fig. 4; column 5, lines 3-10]*;

characterized in that:

the processing elements from the plurality of processing elements are similar to each other, each processing element from the plurality of processing elements being capable of executing each instruction from the plurality of instructions *[column 5, lines 3-10]*; and

the plurality of processing elements are laid out in a regular grid wherein a distance between a processing element and a neighboring processing element from the plurality of processing elements in a first direction is the same as a distance between the processing element and a neighboring processing element from the plurality of processing elements in a second direction that is different from the first direction *[See Fig. 8; column 8, lines 17-21, 31-37]*.

DeHon has not explicitly taught that the issuing means is external to the regular grid.

Mirsky has taught a plurality of processing elements laid out in a regular grid *[Mirsky; array of BFUs or multiple context processing elements (MCPEs); Fig. 1,*

components 102] wherein an issuing means *[Mirsky; configurable instruction decoder; Fig. 1, component 106]* is external to the regular grid *[Mirsky; column 4, lines 46-55].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have modified the integrated circuit of DeHon so that the issuing means is external to the regular grid.

The suggestion/motivation for doing so would have been that the difficulty and expense of decomposing the issuing means into the grid would be alleviated *[Mirsky; column 4, lines 46-55].*

6. Referring to claim 2, DeHon and Mirsky have taught an integrated circuit as claimed in claim 1, wherein the integrated circuit comprises a very long instruction word processor architecture and the subset of the plurality of instructions comprises a very long instruction word *[DeHon; column 5, lines 44-48].*

7. Referring to claim 3, DeHon and Mirsky have taught an integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means connect each processing element to each nearest neighboring processing element in the grid *[DeHon; column 8, lines 23-30].*

8. Referring to claim 4, DeHon and Mirsky have taught an integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means comprise bypassing means for bypassing a processing element from the plurality of processing elements *[DeHon; column 8, lines 38-51].*

9. Referring to claim 5, DeHon and Mirsky have taught an integrated circuit as claimed in claim 1, characterized in that a processing element *[DeHon; BFU]* from the

plurality of processing elements comprises a data storage unit *[DeHon; memory block; Fig. 6, component 110]*, a function unit *[DeHon; ALU core; Fig. 6, component 120]* and an internal intercommunication network *[DeHon; Fig. 6]* coupling the function unit to the data storage unit *[DeHon; olumn 5, line 57 – column 6, line 4]*.

10. Referring to claim 6, DeHon and Mirsky have taught an integrated circuit as claimed in claim 5, characterized in that the processing element comprises at least a further unit *[DeHon; MUX; Fig. 6, component 126]*; the function unit, the further unit and the data storage unit being organized as a very long instruction word processor data path *[DeHon; When the device is configured to be a very long instruction word (VLIW) system, the MUX, the ALU, and the memory block are all part of the a VLIW processor data path (column 5, lines 44-48; Fig. 4)]*.

11. Referring to claim 7, DeHon and Mirsky have taught an integrated circuit as claimed in claim 6, characterized in that the issuing means are distributed over the processing elements *[DeHon; There are multiple F BFUs. Therefore, the issuing means are distributed over the processing elements (BFUs); See Fig. 4; column 5, lines 44-48]*.

12. Referring to claim 8, DeHon and Mirsky have taught a data processing device having an input for receiving a digital data stream and having an output for transmitting a humanly perceptible data result resulting from the digital data stream, characterized in that the input is coupled to the output via an integrated circuit as claimed in claim 1, the integrated circuit being arranged for extracting the data result from the digital data stream *[DeHon; Fig. 22; column 13, lines 49-67]*.

13. Referring to claim 9, given the similarities between claim 1 and claim 9 the arguments as stated for the rejection of claim 1 also apply to claim 9.

14. Referring to claim 10, given the similarities between claim 3 and claim 10 the arguments as stated for the rejection of claim 3 also apply to claim 10.

Response to Arguments

15. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection, which were necessitated by amendment.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER